REMARKS

Claims 1-34 are pending in this application. By this Amendment, claims 1 and 26-28 are amended. Support for the amendments to claims 1, 27 and 28 can be found, for example, in the description of Figs. 5 and 6 and page 18, line 19 - page 25, line 19 of Applicant's specification.

The provisional rejection of claims 1-32 under the judicially created doctrine of obviousness-type double patenting over claims 1, 20 and 21 in co-pending Application No. 09/911,409 has been rendered moot by the cancellation of claims 1, 20 and 21 of co-pending Application No. 09/911,409.

Claims 1-34 were objected to under 37 C.F.R. §1.78(b) as conflicting with claims 1-25 of co-pending Application No. 09/911,409. The objection is respectfully traversed.

Claims 1-34 do not conflict with claims 1-25 of co-pending Application No. 09/911,409 because (1) claims 1, 2, 9, 10 and 17-25 of co-pending Application No. 09/911,409 have been cancelled, (2) claims 3-8 and 11-16 of co-pending Application No. 09/911,409 fail to recite the RAM of amended independent claims 1, 27 and 28 and (3) claims cannot conflict with a co-pending application when the Office Action admits that a provisional rejection under 35 U.S.C. §101 double patenting is improper (the claims admittedly do not recite the same thing). It is respectfully requested that the objection be withdrawn.

Claims 1, 26, 31 and 32 were objected to based on an informality. By this Amendment, all of claims 1, 26, 31 and 32 now recite a microprocessor unit. It is respectfully requested that the objection be withdrawn.

Claims 1, 6, 21, 26, 28, 30, 32 and 34 were rejected under 35 U.S.C. §103(a) over JP 09-281933 (JP'933) in view of Shimamoto, U.S. Patent No. 6,147,472, and claims 27, 29, 31

and 33 were rejected under 35 U.S.C. §103(a) over JP'933 in view Shimamoto and Kida et al. (Kida), U.S. Patent No. 6,335,728. The rejections are respectfully traversed.

None of the applied references disclose or suggest a RAM-incorporated driver with a second control circuit and a RAM that includes memory cells each of which has two input ports through which moving-image data and still-image data are input separately and an output port through which data stored in the memory cell is output, as recited in independent claims 1, 27 and 28.

JP'933 fails to disclose a dual port RAM. JP'933 discloses a data driver where a selector 437 selectively allows (1) the RAM 433 to output stored still-image data and (2) the moving-image data controller (animation controller 311) to output moving-image data. As such, the selector 437 selectively allows the still-image data from the RAM 433 and the moving-image data from the moving-image data controller to be output to the liquid crystal drive circuit (Figs. 2, 3, 6 and 9 and paragraph [0052]). A complicated timing control circuit 411 is required because it is difficult to perform control synchronization for the display control of the screen when moving images and still images are separately stored.

Conversely, the dual port RAM of claims 1, 27 and 28 allows display data to be output from a single output port. As such, the timing at which still-image data and moving-image data are written in the RAM can be independently controlled. Furthermore, it is only necessary for the second control circuit to control the reading of display data of the still-image data or moving-image data that has been stored in the RAM, thereby simplifying the structure of the RAM-incorporated driver.

Shimamoto fails to overcome the deficiencies of JP'933 because Shimamoto fails to disclose the RAM as recited in amended claims 1, 27 and 28. Shimamoto is only relied upon for its reception circuit.

Kida also fails to overcome the deficiencies of JP'933 because Kida fails to disclose or suggest the RAM as recited in amended claims 1, 27 and 28.

In view of the foregoing, none of the applied references disclose or suggest all of the features recited in claims 1, 27 and 28 as well as the additional features recited in the dependent claims thereof. It is respectfully requested that the rejections be withdrawn.

Claims 2-5, 7-10 and 22-25 were rejected under 35 U.S.C. §103(a) over JP'933 in view of Shimamoto and Chida, U.S. Patent No. 6,313,863 and claims 11-20 were rejected under 35 U.S.C. §103(a) over JP'933 in view of Shimamoto and Silverman et al, (Silverman), U.S. Patent No. 6,370,603. The rejections are respectfully traversed.

Chida and Silverman fail to overcome the deficiencies of JP'933 and Shimamoto because Chida and Silverman also fail to disclose the RAM of claims 1, 27 and 28.

Accordingly, none of the applied references disclose or suggest all of the features recited in claims 1, 27 and 28 as well as the additional features recited in claims 2-5, 7-20 and 22-25. It is respectfully requested that the rejections be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-34 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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